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CONFIRMATION

Jun. 10, 2002

SEMICONDUCTOR ENERGY LABORATORY CO., LTD.
ATTN : Ms. Miho KOMORI

Application No.: 90113144
Your ref.: TW4976/4978/4981/4982(T4792)
Our Case: 741062

Dear Sir:

This is in response to your fax dated May 27, 2002.

Enclosed please find the respect copies of Taiwanese Patent Nos. 251379 and 310478 in Chinese.

With respect to Taiwanese Patent No. 310478, we confirm that U.S. Patent 5,943,460 is a corresponding patent thereof by comparing the titles, inventors, assignees, and specifications (including claims and figures) of these two patents.

Finally, we translate the whole specification of Taiwanese Patent No. 251379 as follows:

The manufacture of TFT (Thin Film Transistor) on the glass is a popular solid-state element nowadays. Currently, the TFT manufactured by amorphous silicon (a-Si) has been used for the commercial Liquid Crystal Display (LCD) as a switching element. However, the carrier mobility of amorphous silicon is too low (< 1cm2/V • s), thus it can not be used for manufacturing the peripheral driving circuits. Since the TFT manufactured by polycrystalline silicon (poly-Si) has higher carrier mobility, it will compensate the shortcoming in this aspect and enhance the circuitry characters, product functions and cost efficiency if the poly-Si can be simultaneously manufactured on the glass. However, due to the temperature during the manufacturing process, the development of poly-Si TFT is restrained.

According to the conventional techniques for growing poly-Si thin film (for example, Low Pressure Chemical Vapor Deposition (LPCVD)), the temperature needs to be over 700℃ in order to achieve good quality poly-Si. Even under the lower background pressure (such as 10^{-4} Torr) of the growing chamber, the growing chamber

needs to be over 600℃ to achieve the poly-Si thin film with good crystallinity. Thus it is difficult to achieve growing on the low-cost glass. Besides, the transition temperature between polycrystalline silicon and amorphous silicon is 580℃, thus it is challenging and needs a breakthrough to grow poly-Si thin film below the temperature of 600℃. It has thus become a main object for the industry to develop the process of low temperature poly-Si. For the current techniques, the most common way is to grow amorphous silicon under about 550℃ and go through the furnace annealing (about 550-600℃) for long period of time (generally 1-3 days), so that the poly-Si is obtained. Obviously, such a prolonged method is quite uneconomical, and the time required for the annealing process after ion implantation has not been included yet. So this method is not suitable for industrial production. A desired process is to directly grow good quality poly-Si thin film under low temperature without annealing and without ion implantation, so that the drain and source of low resistance may be obtained, which is accomplished by the present invention.

The main object of the present invention is to provide a simple and efficient process to directly grow the good quality poly-Si, poly-Ge, or poly-SiGe thin film under low temperature without ion implantation, so that the drain and source with excellent low resistance characteristics may be obtained for industrial production.

The present invention discloses a method for manufacturing poly-Si, poly-Ge, or poly-SiGe thin film transistor with low temperature, with the undoped poly-Si layer as a channel layer, by utilizing the methods of the ultrahigh vacuum chemical vapor deposition (UHV/CVD), the low pressure chemical vapor deposition (LPCVD), the molecular beam epitaxy (MBE), or the gas source MBE, especially by the ultrahigh vacuum chemical vapor deposition (UHV/CVD). Thus the good quality poly-Si (SiGe) thin film can be directly grown on a substrate (for example, glass substrate) under low temperature, without any annealing process, to obtain the drain and source with excellent low resistance characteristics, wherein the switch current is above 10^6 and the mobility of field effect electron hole is $28 cm^2/V \bullet sec$. The process employed comprises: providing the undoped poly-Si layer as a channel layer, selectively etching upon the poly-Si to define poly-SiGe, growing high quality poly-Si and poly-SiGe thin film under low temperature by employing the growing method such as the ultrahigh vacuum chemical vapor deposition (UHV/CVD), growing under the extremely low growing pressure (about 1mtorr), and selectively etching the poly-SiGe with the $HF/HNO_3/CH_3COOH$ solution.

As the low pressure chemical vapor deposition is employed, the crystallinity of the thus grown poly-Si and the transition temperature thereof are deeply affected by the growing pressure. When growing is executed under an extremely low pressure, the

crystallinity can be significantly enhanced and the transition temperature thereof is further lowered, thus the poly-Si thin film can be grown on the substrate under low temperature (for example, lower than 600℃).

Furthermore, the present invention may also employ gas source MBE, to grow poly-Si thin film on the substrate under low temperature (for example, lower than 600 ℃).

According to the elements to be formed, the processes of the methods for manufacturing the poly-Si, poly-Ge, or poly-SiGe TFT of the present invention are different, two examples are described as follows:

A. A method for manufacturing poly-Si, poly-Ge, or poly-SiGe thin film transistor above a gate, comprising:

providing the glass as a substrate, wherein said glass is normal glass; depositing low-resistance material above said glass to form a gate, wherein said low-resistance material is a high-temperature resistant metal such as chromium, tungsten, silicified metal; or doped poly-Si (Ge, SiGe); growing 500℃ low-temperature insulation layer (such as silicon oxide or silicon nitride layer) above said gate (2) as a gate dielectric layer; growing undoped poly-Si layer, then growing doped poly-SiGe layer above said poly-Si layer, under the low temperature of 550℃; selectively etching the poly-SiGe layer to form the source and the drain, wherein said selective etching is executed with $HF/HNO_3/CH_3COOH$ solution (such a solution etches the poly-SiGe above the poly-Si with the 10 or more etching rate on the undoped poly-Si layer), and wherein said growing and doping processes is executed under extremely low growing pressure (about 1 mtorr). The doped element can be boron to form a p-type transistor, or can be phosphorous or arsenic to form an n-type transistor.

B. A method for manufacturing poly-Si, poly-Ge, or poly-SiGe thin film transistor under a gate, comprising:

providing the glass as a substrate; growing undoped poly-Si layer, then growing doped poly-SiGe layer, under the low temperature of 550℃; growing a 500℃ low-temperature oxide layer to define the source and the drain area; selectively etching the low-temperature oxide layer above the doped poly-SiGe layer with the BOE solution; and then selectively etching the doped poly-SiGe layer above undoped poly-Si layer to form the source and the drain.

Next, growing the 500℃ low-temperature insulation layer as a gate dielectric layer; depositing low-resistance gate material and defining its area, wherein said selective etching is executed with $HF/HNO_3/CH_3COOH$ solution and the same growing pressure. The doped element can be boron to form a p-type transistor, or can be phosphorous or arsenic to form an n-type transistor.

The present invention will be described in the embodiments with reference to the following drawings.

Fig.1 is an illustrative diagram of the poly-Si TFT above the gate according to present invention.

Fig.2 is an illustrative diagram of the poly-Si TFT under the gate according to present invention.

Four embodiments of the present invention are described as follows:

Embodiment 1:

A method for manufacturing poly-Si thin film transistor above a gate (refer to Fig. 1) comprises the steps of : providing the glass as a substrate 1; depositing a high-temperature resistant and low-resistance metal or doped poly-Si (SiGe) above said glass to form a gate 2 and define the area thereof with the ultrahigh vacuum chemical vapor deposition method, under an extremely low growing pressure (about 0.94 mTorr) and background pressure about 10^{-8} Torr; growing a low-temperature insulation layer 3 above said gate 2 as a gate dielectric layer; wherein the thickness thereof is 30 – 100 nm; growing (under 500℃ - 600℃) an undoped poly-Si layer 4, wherein the growing speed is about 0.66 nm/min and the thickness is 20 - 200 nm; then growing a poly-SiGe layer 5 doped with boron, phosphorous or arsenic, wherein the growing speed is about 2 nm/min and the thickness is 20 - 100 nm; selectively etching the poly-SiGe layer (above the poly-Si layer) to form the source and the drain with $HF/HNO_3/CH_3COOH$ solution. The Si source adopted for deposition is SiH_4 or Si_2H_6 while the Ge source is GeH_4. Under such a low background pressure, the pollutant (such as oxygen) resolved in the deposited thin film will be far less than the lower limit (10^{17} atom/cm2) of the Second Ion Mass Spectro Scopy (SIMS) measures.

Embodiment 2:

A method for manufacturing poly-Si thin film transistor under a gate (refer to Fig. 2), wherein the growing conditions and the Si and Ge sources adopted for deposition are the same as those of Embodiment 1, comprises the steps of : providing the glass as a substrate 1; growing an undoped poly-Si layer 2 of the

thickness 20 – 200 nm above said glass; then growing a poly-SiGe layer 3 (doped with boron, phosphorous or arsenic doped poly-SiGe layer) of the thickness 20 – 200 nm; growing a low-temperature oxide layer 4 of the thickness 200 – 300 nm to define the source and the drain area; etching the low-temperature oxide layer 4 above the poly-SiGe layer3 with the BOE solution; and then selectively etching the poly-SiGe layer 3 above poly-Si layer 2 with $HF/HNO_3/CH_3COOH$ solution to form the source 3 and the drain 3; growing a low-temperature insulation layer 5 as a gate dielectric layer 5 of the thickness 30 – 100 nm; depositing the low-resistance gate material 6 (metal or doped poly-Si (SiGe)) and defining its area.

Embodiment 3:

Adopt the same growing steps and Si and Ge sources as those of Embodiment 1 and Embodiment 2 for manufacturing the TFTs above and under the gate, respectively. The growing method is changed to the low pressure chemical vapor deposition method, the growing pressure is changed as $10^{-2} \sim 10^{-3}$ Torr, and the background pressure is changed as 10^{-4} Torr. The low-temperature growing and doping temperature is now between 500℃ and 600℃. The growing speeds for the poly-Si layer and the poly-SiGe layer are now about 1 nm/min and 2 nm/ min, while the good quality poly-Si layer and poly-SiGe layer are still achieved. Since the higher background pressure is adopted, the vapor or oxygen in the growing chamber will somewhat cause the improper effect on the deposited thin films.

Embodiment 4:

Adopt the same growing steps and Si and Ge sources as those of Embodiment 1 and Embodiment 2 for manufacturing the TFTs above and under the gate, respectively. The growing method is changed to the gas source MBE method, the growing pressure is changed as 10^{-3} Torr, and the background pressure is changed as 10^{-10} Torr. The low-temperature growing and doping temperature is now between 500℃ and 600℃. The growing speeds for the poly-Si layer and the poly-SiGe layer are now about 1 nm/min and 2 nm/ min, while the good quality poly-Si layer and poly-SiGe layer are still achieved.

From the above description, it is understood that the present invention can directly grow good quality poly-Si (Ge, SiGe) thin films with a simple and efficient process, without employing the ion implantation method, so that the drain and source with excellent low resistance characteristics may be obtained for industrial production.

Any modification to the above embodiments can be made by any skilled person in the same field without getting beyond the scope of the attached claims.

Claims

1. A method for manufacturing poly-Si, poly-Ge, or poly-SiGe thin film transistor above a gate, comprising:
   a) providing a glass substrate;
   b) depositing low-resistance material above said substrate to form a gate;
   c) growing low-temperature insulation layer above said gate as a gate dielectric layer;
   d) growing undoped poly-Si, poly-Ge, or poly-SiGe layer above said gate dielectric layer with the ultrahigh vacuum chemical vapor deposition (UHV/CVD), the low pressure chemical vapor deposition (LPCVD) or the gas source MBE, under the temperature of 550℃ or below;
   e) growing doped poly-Si, poly-Ge, or poly-SiGe layer above said undoped poly-Si, poly-Ge, or poly-SiGe layer;
   f) selectively etching said doped poly-Si, poly-Ge, or poly-SiGe layer above said undoped poly-Si, poly-Ge, or poly-SiGe layer to form the source and the drain.
2. The method according to claim 1, wherein said glass is normal glass.
3. The method according to claim 1, wherein said low-resistance material is a high-temperature resistant metal such as chromium, tungsten, silicified metal, etc., or doped poly-Si (Ge, SiGe alloy).
4. The method according to claim 1, wherein the thickness of said gate dielectric layer is 30 – 100 nm.
5. The method according to claim 1, wherein said grown undoped poly-Si, poly-Ge, or poly-SiGe layer has a thickness of 20 – 200 nm.
6. The method according to claim 1, wherein said grown doped poly-Si, poly-Ge, or poly-SiGe layer has a thickness of 20 – 200 nm.
7. The method according to claim 1, wherein said grown undoped poly-Si, poly-Ge, or poly-SiGe layer is a Si layer.
8. The method according to claim 1, wherein said grown undoped poly-Si, poly-Ge, or poly-SiGe layer is a Ge layer.

9. The method according to claim 1, wherein said grown undoped poly-Si, poly-Ge, or poly-SiGe layer is a SiGe layer.

10. The method according to claim 1, wherein said grown doped poly-Si, poly-Ge, or poly-SiGe layer is a Si layer.

11. The method according to claim 1, wherein said grown doped poly-Si, poly-Ge, or poly-SiGe layer is a Ge layer.

12. The method according to claim 1, wherein said grown doped poly-Si, poly-Ge, or poly-SiGe layer is a SiGe layer.

13. The method according to claim 1, wherein said selectively etching of said doped poly-SiGe layer above said undoped poly-Si layer is executed with $HF/HNO_3/CH_3COOH$ solution.

14. The method according to claim 1, wherein the growing method adopted in said step d) is the ultrahigh vacuum chemical vapor deposition (UHV/CVD) method.

15. The method according to claim 14, wherein the outer wall of the heating source is a hotwall when the ultrahigh vacuum chemical vapor deposition (UHV/CVD) method is adopted.

16. The method according to claim 14, wherein the Si source adopted for deposition is SiH_4 or Si_2H_6 while the Ge source is GeH_4 when the ultrahigh vacuum chemical vapor deposition (UHV/CVD) method is adopted.

17. The method according to claim 14, wherein said low-temperature insulation layer is grown under the temperature of 500℃ or less, when the ultrahigh vacuum chemical vapor deposition (UHV/CVD) method is adopted.

18. The method according to claim 14, wherein the low-temperature growing and doping temperature is between 500℃ and 600℃, when the ultrahigh vacuum chemical vapor deposition (UHV/CVD) method is adopted.

19. The method according to claim 14, wherein said growing and doping processes are executed under the extremely low growing pressure of about 1 mTorr and the background pressure of about 10^{-8} Torr, when the ultrahigh vacuum chemical vapor deposition (UHV/CVD) method is adopted.

20. The method according to claim 14, wherein said undoped poly-Si layer is grown with a growing speed of 0.66 nm/min, when the ultrahigh vacuum chemical vapor deposition (UHV/CVD) method is adopted.

21. The method according to claim 14, wherein said doped poly-SiGe layer is grown with a growing speed of 2 nm/min, when the ultrahigh vacuum chemical vapor deposition (UHV/CVD) method is adopted.

22. The method according to claim 1, wherein the growing method adopted in said step d) is the low pressure chemical vapor deposition (LPCVD) method.

23. The method according to claim 22, wherein the outer wall of the heating source is a hotwall when the low pressure chemical vapor deposition (LPCVD) method is adopted.
24. The method according to claim 22, wherein the Si source adopted for deposition is SiH_4 or Si_2H_6 while the Ge source is GeH_4 when the low pressure chemical vapor deposition (LPCVD) method is adopted.
25. The method according to claim 22, wherein said low-temperature insulation layer is grown under the temperature of 500℃ or less, when the low pressure chemical vapor deposition (LPCVD) method is adopted.
26. The method according to claim 22, wherein the low-temperature growing and doping temperature is between 500℃ and 600℃, when the low pressure chemical vapor deposition (LPCVD) method is adopted.
27. The method according to claim 22, wherein said growing and doping processes are executed under the extremely low growing pressure of about $10^{-2} \sim 10^{-3}$ Torr and the background pressure of about 10^{-4} Torr, when the low pressure chemical vapor deposition (LPCVD) method is adopted.
28. The method according to claim 22, wherein said undoped poly-Si layer is grown with a growing speed of 1 m/min and said doped poly-SiGe layer is grown with a growing speed of 2 m/min, when the low pressure chemical vapor deposition (LPCVD) method is adopted.
29. The method according to claim 1, wherein the growing method adopted in said step d) is the gas source MBE method.
30. The method according to claim 29, wherein the outer wall of the heating source is a coldwall when the gas source MBE method is adopted.
31. The method according to claim 29, wherein the Si source adopted for deposition is SiH_4 or Si_2H_6 while the Ge source is GeH_4 when the gas source MBE method is adopted.
32. The method according to claim 29, wherein said low-temperature insulation layer is grown under the temperature of 500℃ or less, when the gas source MBE method is adopted.
33. The method according to claim 29, wherein the low-temperature growing and doping temperature is between 500℃ and 600℃, when the gas source MBE method is adopted.
34. The method according to claim 29, wherein said growing and doping processes are executed under the extremely low growing pressure of about 10^{-3} Torr and the background pressure of about 10^{-10} Torr, when the gas source MBE method is adopted.
35. The method according to claim 1, wherein the ion with the valence of 3 is doped to

manufacture a p-type transistor.

36. The method according to claim 35, wherein said ion with the valence of 3 is the boron.

37. The method according to claim 1, wherein the ion with the valence of 5 is doped to manufacture an n-type transistor.

38. The method according to claim 37, wherein said ion with the valence of 5 is the phosphorous or arsenic.

39. A method for manufacturing poly-Si thin film transistor under a gate, comprising:

a) providing a glass substrate;

b) growing undoped poly-Si, poly-Ge, or poly-SiGe layer above said substrate with the ultrahigh vacuum chemical vapor deposition (UHV/CVD), the low pressure chemical vapor deposition (LPCVD) or the gas source MBE, under the temperature of 550℃ or below;

c) growing doped poly-Si, poly-Ge, or poly-SiGe layer above said undoped poly-Si, poly-Ge, or poly-SiGe layer under low temperature;

d) growing low-temperature oxide layer above said doped poly-Si, poly-Ge, or poly-SiGe layer;

e) etching the low-temperature oxide layer above the doped poly-Si, poly-Ge, or poly-SiGe layer with the BOE solution to define the source and the drain area;

f) selectively etching the doped poly-Si, poly-Ge, or poly-SiGe layer above the undoped poly-Si, poly-Ge, or poly-SiGe layer to form the source and the drain;

g) growing the low-temperature insulation layer as a gate dielectric layer; and

h) depositing the low-resistance gate material and defining its area.

40. The method according to claim 39, wherein said glass is normal glass.

41. The method according to claim 39, wherein said grown undoped poly-Si, poly-Ge, or poly-SiGe layer has a thickness of 20 – 200 nm.

42. The method according to claim 39, wherein said grown doped poly-Si, poly-Ge, or poly-SiGe layer has a thickness of 20 – 100 nm.

43. The method according to claim 39, wherein said grown low-temperature oxide layer has a thickness of 200 – 300 nm.

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44. The method according to claim 39, wherein said grown low-temperature insulation layer as a gate dielectric layer has a thickness of 30 – 100 nm.
45. The method according to claim 39, wherein said grown undoped poly-Si, poly-Ge, or poly-SiGe layer is a Si layer.
46. The method according to claim 39, wherein said grown undoped poly-Si, poly-Ge, or poly-SiGe layer is a Ge layer.
47. The method according to claim 39, wherein said grown undoped poly-Si, poly-Ge, or poly-SiGe layer is a SiGe layer.
48. The method according to claim 39, wherein said grown doped poly-Si, poly-Ge, or poly-SiGe layer is a Si layer.
49. The method according to claim 39, wherein said grown doped poly-Si, poly-Ge, or poly-SiGe layer is a Ge layer.
50. The method according to claim 39, wherein said grown doped poly-Si, poly-Ge, or poly-SiGe layer is a SiGe layer.
51. The method according to claim 39, wherein said selectively etching of said doped poly-SiGe layer above said undoped poly-Si layer is executed with $HF/HNO_3/CH_3COOH$ solution.
52. The method according to claim 39, wherein the ion with the valence of 3 is doped to manufacture a p-type transistor.
53. The method according to claim 52, wherein said ion with the valence of 3 is the boron.
54. The method according to claim 39, wherein the ion with the valence of 5 is doped to manufacture an n-type transistor.
55. The method according to claim 54, wherein said ion with the valence of 5 is the phosphorous or arsenic.

Abstract

A method for manufacturing poly-Si, poly-Ge, or poly-SiGe thin film transistor comprises the steps of: providing the glass as a substrate; depositing the high-temperature resistant and low-resistance metal or doped poly-Si (Ge, SiGe) above said glass to form a gate; growing a low-temperature insulation layer above said gate as a gate dielectric layer with a thickness of about 30 – 100 nm; growing undoped poly-Si, poly-Ge, or poly-SiGe layer with a thickness of about 20 – 200 nm, then growing doped poly-Si, poly-Ge, or poly-SiGe layer with a thickness of about 20 – 200 nm; selectively etching said doped poly-Si, poly-Ge, or poly-SiGe layer above said undoped poly-Si, poly-Ge, or poly-SiGe layer to form the source and the drain with $HF/HNO_3/CH_3COOH$ solution.

Should you have any further questions, please do not hesitate to contact us.

Very Truly Yours,
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WPI Acc No: 1995-282442/199537
XRAM Acc No: C95-127518
Prodn. of polysilicon, germanium or silicon-germanium thin film transistor - under lower temperature and without the implantation
Patent Assignee: GYOSEIIN KOKKA KAGAKU IINKAI (GYOS-N); NAT SCI COMMITTEE
(NASC-N)
Inventor: CHANG J; LIN H; LIN S
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
TW 251379	A	19950711	TW 94100725	A	19940128	199537	B
JP 8023099	A	19960123	JP 9442274	A	19940314	199613	N

Priority Applications (No Type Date): TW 94100725 A 19940128; JP 9442274 A 19940314
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
TW 251379	A		20	H01L-021/331	
JP 8023099	A		5	H01L-029/786	

Abstract (Basic): TW 251379 A

Prodn. of polysilicon, Ge or Si-Ge thin film transistor with gate on the down side includes: (a) supplying a glass as substrate; (b) depositing the material with low resistance on the substrate to form gate; (c) growing low-temperature insulator on the gate as gate dielectric layer; (d) growing undated polysilicon, Ge or Si-Ge layer on gate dielectric layer with UHV/CVD, LPCVD or gas source MBE and below 550 deg. C; (d) growing doped polysilicon, Ge or Si-Ge layer on undoped polysilicon, Ge or Si-Ge layer; and (e) selectively etching the doped polysilicon, Ge or Si-Ge layer on the undoped polysilicon, Ge or Si-Ge layer to form source and drain.

Dwg.0/2

Title Terms: PRODUCE; POLY; SILICON; GERMANIUM; SILICON; GERMANIUM; THIN;
FILM; TRANSISTOR; LOWER; TEMPERATURE; IMPLANT
Derwent Class: L03; U11; U14
International Patent Class (Main): H01L-021/331; H01L-029/786
International Patent Class (Additional): H01L-021/336

File Segment: CPI; EPI

附件

公告本

251379

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類別	H01L 21/331

（以上各欄由本局填註）

83年11月10 修正 A4 補充 C4

發明／新型 專利說明書

一、發明／新型名稱	中文	多晶矽、鍺、或矽鍺薄膜電晶體之製造方法(83年11月修正本)
	英文	
二、發明／創作人	姓名	1. 張俊彥　3. 林孝義 2. 林鴻志
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	國籍	中華民國
	住、居所（事務所）	台北市和平東路二段106號18樓
	代表人姓名	郭南宏

裝　訂　線

經濟部中央標準局員工消費合作社印製

本紙張尺度適用中國國家標準（CNS）A4規格（210×297公釐）

251379

A8
B8
C8
D8

六、申請專利範圍

修正
84年3月22日
補充

（第83100725號申請案申請專利範圍84年3月修正本）

1．一種閘極在下之多晶矽、鍺、或矽鍺薄膜電晶體之製造方法，其包括：

a）提供一玻璃作為基板；

b）令低阻值之物質沉積於該基板形成閘極；

c）使於該閘極上成長低溫絕緣層做為閘極介電層；

d）以超高真空化學氣相沉積法（UHV/CVD）、低壓化學氣相沉積法（LPCVD）或氣相源分子束磊晶法（Gas Source MBE）於550℃以下，於該閘極介電層上成長未摻雜之多晶矽、鍺、或矽鍺層；

e）於該未摻雜之多晶矽、鍺、或矽鍺層上成長摻雜之多晶矽、鍺、或矽鍺層；以及

f）於該未摻雜之多晶矽、鍺、或矽鍺層上，選擇性蝕刻該摻雜多晶矽、鍺、或矽鍺層，形成源極與汲極（source and drain）。

2．如申請專利範圍第1項所述之製造方法，其中該玻璃係一般常見之玻璃。

3．如申請專利範圍第1項所述之製造方法，其中該低阻值之物質係耐高溫金屬（如鉻，鎢，矽化金屬等）或摻雜之多晶矽、鍺、矽鍺合金。

4．如申請專利範圍第1項所述之製造方法，其中該閘極介電層其厚度為30－100nm。

5．如申請專利範圍第1項所述之製造方法，其中該成長未摻雜之多晶矽、鍺、或矽鍺層，其厚度為20－200nm。

（請先閱讀背面之注意事項再填寫本頁）

訂

經濟部中央標準局員工消費合作社印製

六、申請專利範圍

6．如申請專利範圍第1項所述之製造方法，其中該再成長摻雜之多晶矽、鍺、或矽鍺層，其厚度爲20-100nm。

7．如申請專利範圍第1項所述之製造方法，其中該成長未摻雜之多晶矽、鍺、或矽鍺層係矽層。

8．如申請專利範圍第1項所述之製造方法，其中該成長未摻雜之多晶矽、鍺、或矽鍺層係鍺層。

9．如申請專利範圍第1項所述之製造方法，其中該成長未摻雜之多晶矽、鍺、或矽鍺層係矽鍺層。

10．如申請專利範圍第1項所述之製造方法，其中該再成長摻雜之多晶矽、鍺、或矽鍺層係矽層。

11．如申請專利範圍第1項所述之製造方法，其中該再成長摻雜之多晶矽、鍺、或矽鍺層係鍺層。

12．如申請專利範圍第1項所述之製造方法，其中該再成長摻雜之多晶矽、鍺、或矽鍺層係矽鍺層。

13．如申請專利範圍第1項所述之製造方法，其中該選擇性蝕刻摻雜之多晶矽鍺層於未摻雜之多晶矽層上，係以$HF/HNO_3/CH_3COOH$完成之。

14．如申請專利範圍第1項所述之製造方法，其中於該步驟(d)中所使用之成長方法係可爲超高真空化學氣相沉積法(UHV/CVD)。

15．如申請專利範圍第14項所述之製造方法，其中使用該超高真空化學氣相沉積法時，加熱源之外壁係爲一熱壁(hotwall)。

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六、申請專利範圍

１６．如申請專利範圍第１４項所述之製造方法，其中使用該超高真空化學氣相沉積法時，所使用之矽源材（Si source）係爲SiH_4或Si_2H_6，鍺源材（Ge source）係爲GeH_4。

１７．如申請專利範圍第１４項所述之製造方法，其中使用該超高真空化學氣相沉積法時，該低溫絕緣層係於低於５００℃下成長。

１８．如申請專利範圍第１４項所述之製造方法，其中使用該超高真空化學氣相沉積法時，其低溫成長及摻雜溫度係介於５００℃～６００℃。

１９．如申請專利範圍第１４項所述之製造方法，其中使用該超高真空化學氣相沉積法時，該成長及摻雜過程係以極低成長壓力約１mTorr及背景壓力10^{-8}Torr下進行。

２０．如申請專利範圍第１４項所述之製造方法，其中使用該超高真空化學氣相沉積法時，係以0.66nm/min之成長速度，成長該未摻雜之多晶矽層。

２１．如申請專利範圍第１４項所述之製造方法，其中使用該超高真空化學氣相沉積法時，係以2nm/min之成長速度，成長該摻雜之多晶矽鍺層。

２２．如申請專利範圍第１項所述之製造方法，其中於該步驟（d）中所使用之成長方法係可爲低壓化學氣相沉積法（LPCVD）。

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六、申請專利範圍

２３．如申請專利範圍第２２項所述之製造方法，其中使用該低壓化學氣相沉積法時，加熱源之外壁係為一熱壁(hotwall)。

２４．如申請專利範圍第２２項所述之製造方法，其中使用該低壓化學氣相沉積法時，所使用之矽源材(Si source)係為SiH_4或Si_2H_6，鍺源材(Ge source)係為GeH_4。

２５．如申請專利範圍第２２項所述之製造方法，其中使用該低壓化學氣相沉積法時，該低溫絕緣層係於低於５００℃下成長。

２６．如申請專利範圍第２２項所述之製造方法，其中使用該低壓化學氣相沉積法時，其低溫成長及摻雜溫度係介於５００℃～６００℃。

２７．如申請專利範圍第２２項所述之製造方法，其中使用該低壓化學氣相沉積法時，該成長及摻雜過程係以極低成長壓力約10^{-2}～10^{-3}Torr及背景壓力約10^{-4}Torr下進行。

２８．如申請專利範圍第２２項所述之製造方法，其中使用該低壓化學氣相沉積法時，係以１m/minの成長速度，成長該未摻雜之多晶矽層以及以２m/min之成長速度，成長該摻雜之多晶矽鍺層。

２９．如申請專利範圍第１項所述之製造方法，其中於該步驟(d)中所使用之成長方法係可為氣相源分子束磊晶法(Gas Source MBE)。

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六、申請專利範圍

３０．如申請專利範圍第２９項所述之製造方法，其中使用該氣相源分子束磊晶法時，加熱源之外壁係為一冷壁（ｃｏｌｄｗａｌｌ）。

３１．如申請專利範圍第２９項所述之製造方法，其中使用該氣相源分子束磊晶法時，所使用之矽源材（Ｓｉ ｓｏｕｒｃｅ）係爲SiH_4或Si_2H_6，鍺源材（Ｇｅ ｓｏｕｒｃｅ）係爲GeH_4。

３２．如申請專利範圍第２９項所述之製造方法，其中使用該氣相源分子束磊晶法時，該低溫絕緣層係於低於５００℃下成長。

３３．如申請專利範圍第２９項所述之製造方法，其中使用該氣相源分子束磊晶法時，其低溫成長及摻雜溫度係介於５００℃～６００℃。

３４．如申請專利範圍第２９項所述之製造方法，其中使用該氣相源分子束磊晶法時，該成長及摻雜過程係以極低成長壓力約10^{-3}Ｔｏｒｒ及背景壓力約10^{-10}Ｔｏｒｒ下進行下進行。

３５．如申請專利範圍第１項所述之製造方法，其中係摻雜三價之離子而製造成一ｐ ｔｙｐｅ電晶體。

３６．如申請專利範圍第３５項所述之製造方法，該三價之離子係硼。

３７．如申請專利範圍第１項所述之製造方法，其中係摻雜五價之離子而製造成一ｎ－ｔｙｐｅ電晶體。

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六、申請專利範圍

３８．如申請專利範圍第３７項所述之製造方法，該五價之離子係磷或砷。

３９．一種閘極在上之多晶矽薄膜電晶體之製造方法，其包括：

a)提供一玻璃作爲基板；

b)以超高真空化學氣相沉積法(UHV/CVD)、低壓化學氣相沉積法(LPCVD)或氣相源分子束磊晶法(Gas Source MBE)於550℃以下，於該基板上成長未摻雜之多晶矽、鍺、或矽鍺層；

c)使於該未摻雜之多晶矽、鍺、或矽鍺層上再低溫成長摻雜之多晶矽、鍺、或矽鍺層；

d)使於該摻雜之多晶矽、鍺、或矽鍺層上再成長低溫氧化層；

e)定義源極與汲極(source and drain)，先以BOE溶液於摻雜之多晶矽、鍺、或矽鍺層上蝕刻低溫氧化層；

f)於未摻雜之多晶矽、鍺、或矽鍺層上選擇性蝕刻摻雜之多晶矽、鍺、或矽鍺層，使形成源極與汲極。

g)成長低溫絕緣層，以作爲閘極介電層；以及

h)沉積低阻値之閘極材質並定義其區域。

４０．如申請專利範圍第３９項所述之製造方法，其中該玻璃係一般常見之玻璃。

４１．如申請專利範圍第３９項所述之製造方法，其中該成長未摻雜之多晶矽、鍺、或矽鍺層，其厚度爲20－200nm。

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六、申請專利範圍

４２．如申請專利範圍第３９項所述之製造方法，其中該再成長摻雜之多晶矽、鍺、或矽鍺層，其厚度為20-100nm。

４３．如申請專利範圍第３９項所述之製造方法，其中該成長低溫氧化層，其厚度為200-300nm。

４４．如申請專利範圍第３９項所述之製造方法，其中該成長低溫絕緣層，以作為閘極介電層其厚度為30-100nm。

４５．如申請專利範圍第３９項所述之製造方法，其中該成長未摻雜之多晶矽、鍺、或矽鍺層係矽層。

４６．如申請專利範圍第３９項所述之製造方法，其中該成長未摻雜之多晶矽、鍺、或矽鍺層係鍺層。

４７．如申請專利範圍第３９項所述之製造方法，其中該成長未摻雜之多晶矽、鍺、或矽鍺層係矽鍺層。

４８．如申請專利範圍第３９項所述之製造方法，其中該再成長摻雜之多晶矽、鍺、或矽鍺層係矽層。

４９．如申請專利範圍第３９項所述之製造方法，其中該再成長摻雜之多晶矽、鍺、或矽鍺層係鍺層。

５０．如申請專利範圍第３９項所述之製造方法，其中該再成長摻雜之多晶矽、鍺、或矽鍺層係矽鍺層。

５１．如申請專利範圍第３９項所述之製造方法，其中該選擇性蝕刻摻雜之多晶矽鍺層於未摻雜之多晶矽層上，係以$HF/HNO_3/CH_3COOH$完成之。

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六、申請專利範圍

５２．如申請專利範圍第３９項所述之製造方法，其中係摻雜三價之離子而製造成一p type電晶體。

５３．如申請專利範圍第５２項所述之製造方法，該三價之離子係硼。

５４．如申請專利範圍第３９項所述之製造方法，其中係摻雜五價之離子而製造成一n type電晶體。

５５．如申請專利範圍第５４項所述之製造方法，該五價之離子係磷或砷。

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五、發明說明(1)

在玻璃上製造薄膜電晶體(Thin Film Transistor,簡稱TFT),乃現今非常熱門之一種固態元件，目前利用非晶矽(amorphous silicon,簡稱a-Si)製成之 TFT已被用於商業化之液晶顯示螢幕(Liquid Crystal Display,簡稱LCD)中作爲開關切換元件,然由於非晶矽之載子遷移率(Carrier Mobility)太低(<$1cm^2/V\cdot s$),故不能用於製作週邊之驅動電路,然以多晶矽製成之薄膜電晶體,則擁有較高之載子遷移率(>$10cm^2/V\cdot s$),故可彌補非晶矽薄膜電晶體在此方面之不足,如能將多晶矽薄膜電晶體同時製造於玻璃上,對電路特性,產品功能及成本都有莫大之助益,但由於在製程中溫度緣故,限制了多晶矽薄膜電晶體在此方面之發展。

就傳統之成長多晶矽薄膜之技術 (如低壓化學氣相沉積法LPCVD)而言,要獲得良好品質之多晶矽,其溫度往往超過700℃,即使在較低之成長室的背景壓力如10^{-4}Torr爲之，仍必須在大於600℃之成長溫度下，方能獲得結晶性良好之多晶矽薄膜，故難以成長在低成本之玻璃上,況且多晶矽與非晶矽之轉移溫度(transition temperature)的爲580℃，要在600℃以下成長多晶矽薄膜，極具挑戰性而有待突破，所以需發展低溫化多晶矽之製程(<600℃),成爲各方努力之方向,就目前之技術而言,最常爲採用之方式,乃首先於約550℃成長非晶矽,而後經由長時間(一般約1-3天)之爐管退火處理(約550-600℃),使其晶化生成多晶矽,很明顯,此種曠日費時之方

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五、發明說明（ 2 ）

法甚不經濟，而且這還不包括離子佈植後之退火處理所需時間，故，此法不適合於工業上之生產。然較理想之製程即於低溫下直接成長良好品質之多晶矽薄膜，不必退火，同時不利用離子佈植的方法，即可獲致低阻值之汲極與源極（drain and source），而本案即可達到上述之目的。

本案之主要目的爲以一種簡單而有效率之製程，而可於低溫下直接成長良好品質之多晶矽、鍺、或矽鍺薄膜，同時不利用離子佈植的方法，即可獲致低阻值特性甚佳之汲極與源極，以適合工業上之生產。

本案爲一種以低溫製造多晶矽、鍺、或矽鍺薄膜電晶體之製造方法，其主要觀念是以未摻雜之多晶矽層（undoped poly-Si layer）爲通道層（channel layer），其係利用超高眞空化學氣相沉積法（UHV/CVD）、低壓化學氣相沈積法（LPCVD）、分子束磊晶法（MBE），或氣相源分子束磊晶法（Gas Source MBE），尤其是利用超高眞空化學氣相沉積法（UHV/CVD），故可於低溫下，於一基板上，如玻璃基板，直接成長良好品質之多晶矽（矽鍺）薄膜，且不需任何之退火處理，即可獲致低阻值特性甚佳之汲極與源極，開關電流比大於10^8以上，場效電洞遷移率達$28cm^2/V\cdot sec$。而其形成手段爲令未摻雜之多晶矽層爲通道層、於多晶矽上以選擇性蝕刻（selective etching）定義多晶矽鍺、利用超高眞空化學氣相沉積法（UHV/CVD）等成長方法低溫成長高品質poly-Si及poly-SiGe薄膜、以極低

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五、發明說明（ 3 ）

成長壓力（約 1mtorr）下進行成長．利用 $HF/HNO_3/CH_3COOH$ 溶液選擇性蝕刻多晶矽鍺。

若是採用低壓化學氣相沈積法，所成長多晶矽之結晶性及其轉變溫度（Transition Temperature）係深受成長壓力之影響，當在一極低壓力下成長，其結晶性可大幅提升而其轉變溫度會更加降低，因此亦可在低溫下（如低於600℃下）於基板上成長多晶矽薄膜。

另外，本案亦可採用氣相源分子束磊晶法（Gas Source MBE），在低溫下（如低於600℃下）於基板上成長多晶矽薄膜。

本案多晶矽、鍺、或矽鍺薄膜電晶體之製造方法，然因欲形成之元件不同，而處理之程序亦有不同，現舉二例述之如下：

A．閘極在下之多晶矽薄膜電晶體之製造方法；

以一玻璃作爲基板，該玻璃爲普通玻璃，令低阻值之物質，沉積於該玻璃形成閘極，而該低阻值之物質，係耐高溫之金屬如鉻，鎢，矽化金屬等或摻雜之多晶矽（鍺、矽鍺），使於其上成長500℃低溫絕緣層（如氧化矽或氮化矽層）做爲閘極介電層，續以550℃之低溫成長未摻雜之多晶矽層，再成長摻雜之多晶矽鍺層，於該多晶矽層上，選擇性蝕刻多晶矽鍺層，形成源極與汲極（source and drain），該選擇性蝕刻係以 $HF/HNO_3/CH_3COOH$ 完成（此液蝕刻多晶矽鍺於多晶矽上，對未摻雜多晶矽層之蝕刻率比可達10以上），而其中該成長及摻雜過程係以極低成長壓力（約

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五、發明説明（ 4 ）

1mtorr）下成長。摻雜之元素可爲硼而形成p-type電晶體，或可爲磷、砷而形成n-type電晶體。

B.閘極在上之多晶矽薄膜電晶體之製造方法；

以一玻璃作爲基板，於其上以550℃之低溫成長未摻雜之多晶矽層，再成長摻雜之多晶矽鍺層，使於其上成長500℃低溫氧化層，定義源極與汲極區域，先以BOE溶液於摻雜之多晶矽鍺層上蝕刻低溫氧化層，再於未摻雜之多晶矽層上選擇性蝕刻摻雜多晶矽鍺層，使形成源極與汲極。

接著成長500℃低溫絕緣層，以作爲閘極介電層，沉積低阻値之閘極材質並定義其區域，該選擇性蝕刻係以$HF/HNO_3/CH_3COOH$完成之，成長壓力亦然。摻雜之元素亦可爲硼而形成p-type電晶體，或可爲磷、砷而形成n-type電晶體。

爲易於說明，本案得藉下述之較佳實施例及圖示以求更佳了解。

第一圖：係本案閘極在下多晶矽薄膜電晶體之示意圖。

第二圖：係本案閘極在上多晶矽薄膜電晶體之示意圖。

本案因欲形成之元件不同，而處理之程序亦有不同，現舉四較佳實施例述之如下：

實施例一：

一種閘極在下之多晶矽薄膜電晶體之製造方法，請參閱第一圖，其係以一玻璃作爲基板1，以極低成長壓力（約

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五、發明說明（5）

0.94mTorr)及背景壓力約10^{-8}Torr下並以超高真空化學氣相沉積法，於其上以耐高溫低阻值之金屬或摻雜之多晶矽(矽鍺)沉積於該玻璃形成閘極2，並定義其區域，使於其上成長低溫絕緣層3做爲閘極介電層，其厚度爲30-100nm，於約500～600℃下成長未摻雜之多晶矽層4，成長速度可約爲0.66nm/min，其厚度爲20-200nm，再成長摻雜硼、磷、或砷之多晶矽鍺層5，成長速度可約爲2nm/min，其厚度爲20-100nm，利用$HF/HNO_3/CH_3COOH$溶液，於多晶矽層上，選擇性蝕刻多晶矽鍺層，形成源極與汲極(source and drain)；於沈積時所使用之矽源材(Si source)係爲SiH_4或Si_2H_6，鍺源材(Ge source)係爲GeH_4，且由於在如此低之背景壓力下，沈積薄膜內所溶併之污染物，如氧氣之濃度將已遠低於二次離子質譜分析(Second Ion Mass Spectro Scopy SIMS)偵測度之下限(10^{17}原子$/cm^2$)。

實施例二：

一種閘極在上之多晶矽薄膜電晶體之製造方法，請參閱第二圖，成長條件及沈積時所使用之矽、鍺源材係同實施例一，其係以一玻璃作爲基板1，於其上成長未摻雜之多晶矽層2，其厚度爲20-200nm，再成長摻雜硼、磷、或砷之多晶矽鍺層3，其厚度爲20-100nm，使於其上成長低溫氧化層4，其厚度爲200-300nm，定義源極與汲極，先以BOE溶液於多晶矽鍺層3上蝕刻低溫氧化層4，再利用

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五、發明説明(6)

$HF/HNO_3/CH_3COOH$溶液，於多晶矽層2上選擇性蝕刻多晶矽鍺層3，使形成源極3與汲極3，成長低溫絕緣層5，以作爲閘極介電層5，其厚度爲30-100nm，沉積低阻值之閘極材質6〔金屬或摻雜之多晶矽(矽鍺)〕並定義其區域。

實施例三：

成長步驟及矽、鍺源材同實施例一及二分別製造閘極在下及在上之薄膜電晶體，然成長方式改採低壓化學氣相沈積法，且成長條件中成長壓力改爲10^{-2}～10^{-3}Torr，背景壓力改爲10^{-4}Torr，低溫成長及摻雜溫度則係介於500℃～600℃間，以及多晶矽及矽鍺層之成長速度分別約爲1nm/min及2nm/min時，仍可獲得良好之多晶矽及矽鍺層，但因採用較高之背景壓力，因此成長室內之水汽或氧氣會多少對沈積之薄膜造成不良影響。

實施例四：

成長步驟及矽、鍺源材同實施例一及二分別製造閘極在下及在上之薄膜電晶體，然成長方式改採氣相源分子束磊晶法(Gas Source MBE)，且成長條件中成長壓力爲10^{-3}Torr、背景壓力改爲10^{-10}Torr，低溫成長及摻雜溫度則係介於500℃～600℃間，以及多晶矽及矽鍺層之成長速度分別約爲1nm/min及2nm/min時，仍可獲得良好之多晶矽及矽鍺層

由上之所述可知，本案確可以一種簡單而有效率之製程，於低溫下直接成長良好品質之多晶矽(鍺、矽鍺)薄膜，同時不利用離子佈植的方法，即可獲致低阻值特性甚佳之

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五、發明說明（ 7 ）

汲極與源極，以適合工業上之生產，凡熟悉本技藝人士得任施匠思而爲諸般修飾，然皆不脫如附申請專利範圍所欲保護者。

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四、中文發明摘要（發明之名稱：　　　　　　　　　　　　）

多晶矽、鍺、或矽鍺薄膜電晶體之製造方法

一種多晶矽、鍺、或矽鍺薄膜電晶體之製造方法，其係以一玻璃作爲基板，次以耐高溫低阻值之金屬或摻雜之多晶矽（鍺、矽鍺）沉積於該玻璃形成閘極，再於其上使形成低溫絕緣層做爲閘極介電層，其厚度約爲30－100nm，再成長未摻雜之多晶矽、鍺、或矽鍺層，其厚度約爲20－200nm，後再成長摻雜之多晶矽、鍺、或矽鍺層，其厚度約爲20－100nm，然後利用$HF/HNO_3/CH_3COOH$溶液，於該未摻雜之多晶矽、鍺、或矽鍺層上，選擇性蝕刻該摻雜之多晶矽、鍺、或矽鍺層，以形成源極與汲極。

英文發明摘要（發明之名稱：　　　　　　　　　　　　）

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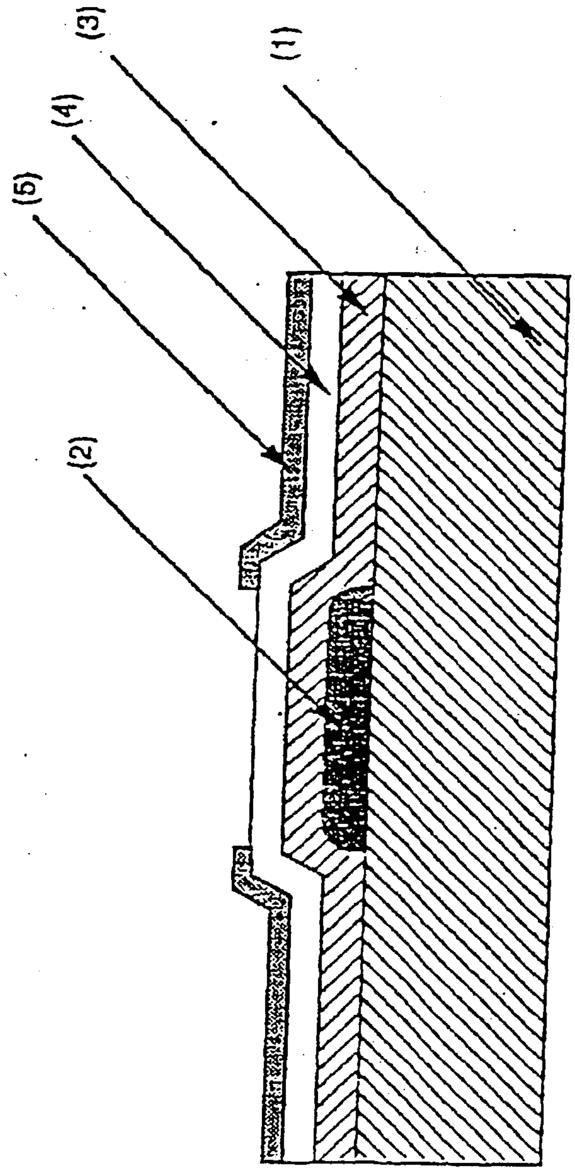
圖式



第一圖

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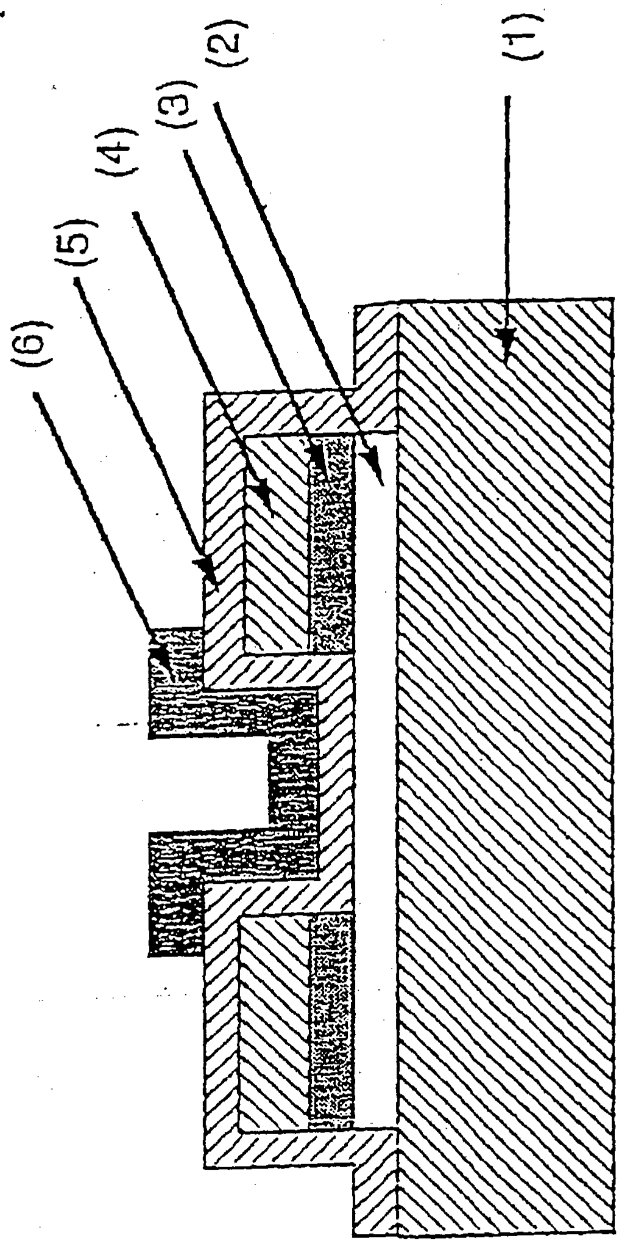

第二圖

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